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An ion track based approach to nano- and micro-electronics

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Abstract

Since a decade the concept emerged to use conducting ion tracks in nano- and micro-electronics, due to their small dimensions. Whereas in a few cases the ion tracks themselves are already conducting, in the majority of all cases the ion tracks have first to be etched to form nanopores, into which (semi)conducting matter is inserted thereafter. The MOS-type hybrid structures "TEAMS" and "TEMPOS", consisting of silicon/insulator bilayer systems into which such conducting tracks had been inserted and which are eventually combined with nanoclusters (NCs), NC/polymer composites or carbon nanotubes, have proven to be of special electronic interest due to their great versatility. Electronic elements based on this concept combine many peculiar properties such as negative differential resistances (NDR), sensing, AND/OR logics and light emission in an unconventional way. For demonstration purpose, NDRs were used for signal amplification up to a factor 24. Network theory has been used to estimate the minimum possible size of these structures and the geometrical distributions of the internal current flows. Suitably tailored electronic circuits make use of these structures for practical applications.
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1. Introduction: swift-heavy ion track electronics

The impact of energetic heavy ions onto insulators yields long ($10 to 100 lm) and narrow ($1 to 10 nm) trails of excessive damage, the so-called latent ion tracks. In some targets – e.g. organometals, metal oxides, polysilanes, diamond and fullerite – these latent tracks are (semi)conducting due to the radiation-induced formation of metals, metal oxides, sulfides, SiC, or sp2-enriched carbonaceous fragments, respectively. Otherwise, conducting nanowires can be formed by track etching and subsequent insertion of solid (semi)conducting solids into the thus created nanopores. Passive and active electronic elements such as resistors, capacitors, inductors, sensors, transformers, normal and light emitting diodes and field effect transistors have already been made with these elements [1,2]. This family of electronic elements had been denoted as "Swift-heavy Ion Track Electronics" (SITE) [3–5]. It is also possible to insert electrolytes into etched tracks in polymeric membranes which may give rise to a biomimetic "Electrolytic Electronics with Etched Tracks" (E_3T) [6–8].

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2. TEAMS and TEMPOS

There have also been developed some other SITE structures "TEAMS" [9] and "TEMPOS" [10–13] which are based on MOS-type semiconductor/insulator hybrides. The acronym "TEAMS" stands for "Tuneable Electronically Anisotropic Materials on Semiconductors", pointing at the strong anisotropy of the irradiated layers which had been imposed onto them by the parallel ion tracks. "TEMPOS" stands for "Tuneable Electronic Material inserted intoPores in Oxide on Semiconductors", as the most prominent track-bearing materials in this field have hitherto been silicon oxides. These structures, preferentially mounted onto silicon substrates, are advantageous as they can be readily integrated into conventional electronics. Any (semi)conducting materials can be used for the construction of TEAMS and TEMPOS structures such as metals, semiconductors, conducting polymers, organometals, metal/polymer or semiconductor/polymer nanocompounds and solid or liquid electrolytes, so that the structures can be easily tailored to obtain the desired properties, e.g. for physical and chemical sensors. Additionally, they show the capability for multiparametric logic decision-making.

For the following consideration let us restrict for simplicity to a TEMPOS structure with a high-Ohmic layer of metallic (e.g. Ag) NCs covering both the inner walls of the etched tracks and the surface of the SiO_2 dielectric layer on a p-Si substrate, as was described earlier in [10]. The top layer is contacted by two electrodes o and w, and the semiconductor substrate by another electrode (v) on the rear side. The metal–silicon band transition within the etched tracks behaves like a diode. Underneath the oxide, there might exist an accumulation, depletion or inversion layer. Next to the applied biases, the existence of such a layer (channel) depends on the leakage properties of the oxide represented by the track resistance R_t and the diode properties D_{ox}, R_{ox}. This channel has a direct analogue in the channel between source and drain of a MOS transistor.

Due to the similarity of MOS and TEMPOS structures, one can just use a modified theory of MOS transistors [14] to describe TEMPOS electronics. However, for a straightforward calculation the highly complicated equivalent circuit of such a structure (Fig. 1(a)) has first to be simplified by restricting to 2 conducting tracks only that are directly connected to the electrodes o and w, Fig. 1(b), Then one can calculate the voltage V along the interface channel, to obtain the drain current I_o (i.e. the current between the two surface contacts of a TEAMS/ TEMPOS structure) by differentiation

$$I_o = \iint j(x,y)\,dx\,dz = W\mu(-dV_c/dy)\,n(x,y)\,dx; \quad (1)$$

where x defines the track direction, y describes the direction along the channel, and z points along the channel width. W is the channel width, V_c is the voltage along that channel

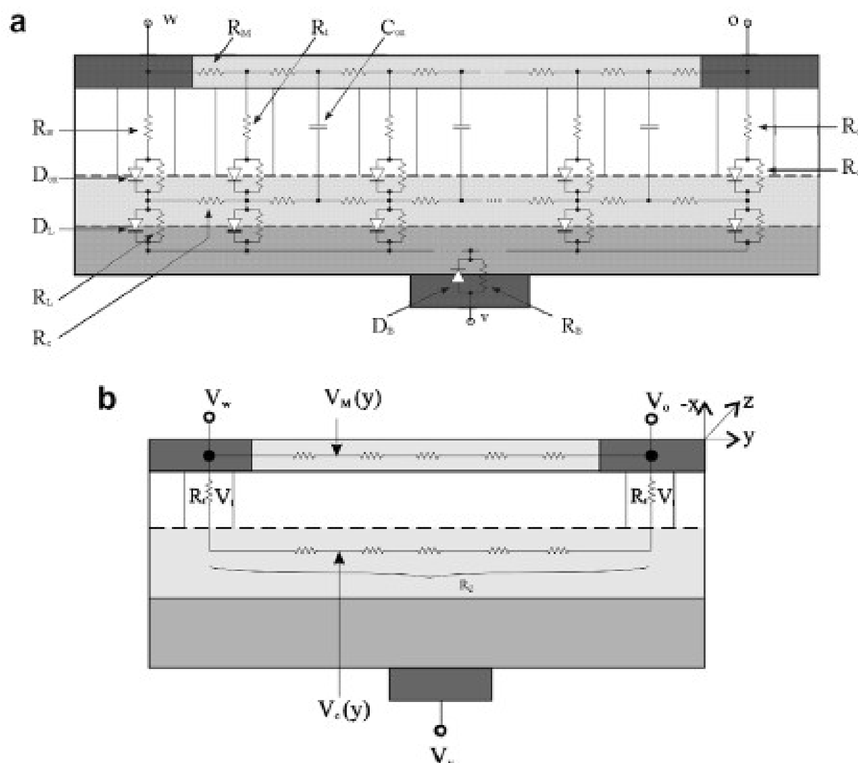

Fig. 1. Equivalent circuits of a TEMPOS structure, (a) complete, (b) simplified circuit. R denotes resistances, C capacities, D diodes and V the applied potentials. The indices o, v, w refer to the three corresponding contacts; the indices t, ox, M, L and c stand for the tracks, the oxide layer, the highly resistive surface layer, the transition region between the bulk silicon and the interface-near conducting channel, and that channel itself, respectively.

and l is the mobility within the channel. The integral on the right side is the surface charge density r(y), related to the oxide field by r(y) = $e_{ox}E_{ox}$ with E_{ox} = DV/d_{ox}, d_{ox} being the thickness and e_{ox} being the dielectric coefficient of the oxide layer. This allows one to calculate DV. After insertion and integration, one obtains an expression for the drain current

$$I_o = b(R/(R+2))(V_v + V_w)(V_o - V_w) \quad (2)$$

with b = C_{ox}l W/L, C_{ox} being the capacity per unit area of the oxide layer, L being the channel length, and R being the ratio of channel to track resistance R = R_c/R_t. This expression is only valid for small V_{ow}; for higher V_{ow} Eq. (2) approaches to the classical description of a MOS transistor. In other words, MOS transistors can be regarded as a special case of TEMPOS structures.

3. Amplification and negative differential resistances

Due to this result, it is not surprising that also TEMPOS structures show the characteristic properties of transistors such as the capabilities for amplification and switching. Therefore we may identify the terminals w, o, v as emitter, base and collector, respectively.

Consider Fig. 2 which shows the characteristics of the Ag NCs TEMPOS structure described above [10]. The highlighted region indicates the current/voltage regime within which power amplification was found, Table 1. The measurement points A, B, . . . , E in this table correspond to the working points described in Fig. 2. This region is characterized by slightly noisy curve shapes, a more detailed inspection showing micropulsations with negative differential resistances (NDRs). These micropulsations are accompanied by spark-like light emission at all visible wavelengths, which are tentatively attributed to phonon emission associated to electron hopping between the Ag nanoclusters embedded in the etched tracks.

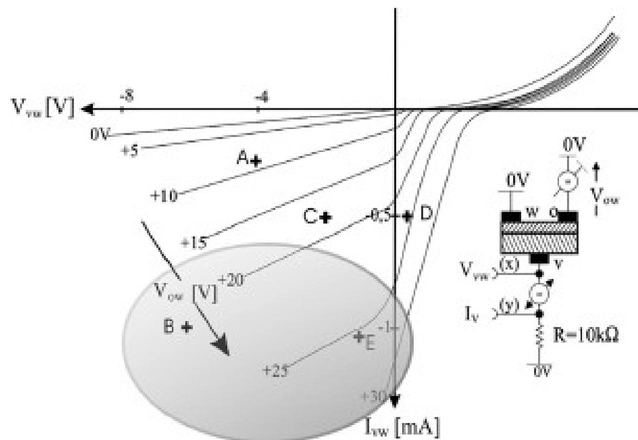

Fig. 2. Typical characteristic of a Ag-NC-TEMPOS structure. The highlighted region renders amplification. Curves smoothed-out for the sake of simplicity.

Table 1
Power amplification of a Ag-NC-TEMPOS structure at high currents

Examined point	Common emitter	Common base	Common collector
B	1.17	0.12	24
E	0.053	1.12	0.074

The points B and E refer to the highlighted region of Fig. 1. The other points A, C and D show amplifications <1.

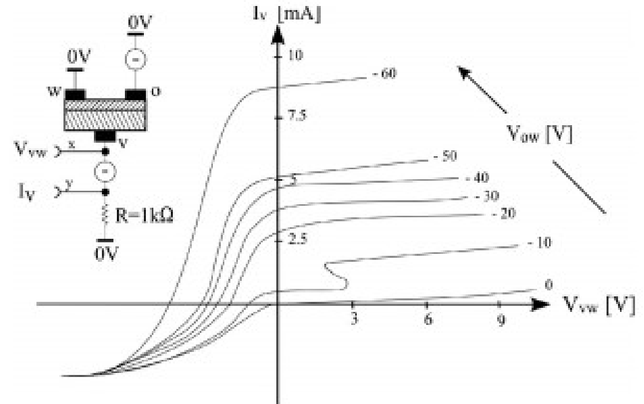

Fig. 3. Characteristic of a Ag-NC-TEMPOS structure with NDR under specific working conditions.

Occasionally these NDRs show up more pronouncedly as illustrated in Fig. 3. This behavior has been explained [15] by the interaction of neighbored tracks A and B, with the track-to-track distance being less than the mean free charge carrier pathlength k in the conducting channel. Under this condition one can influence the working state of an ion track diode D_A by its neighboring diode D_B. This is accomplished e.g. by injecting charge carriers into the interface channel region below the closed ion track diode D_A via a neighboring conducting track diode D_B which had been put onto a sufficiently high potential. If properly tailored, the previously closed diode D_A will then open, thus allowing more charge carriers to flow into the conducting interface channel, and thereby triggering other neighbored track diodes to open, too. This avalanche process leads to an abrupt jump from a high-Ohmic working state of charge occupancy in the whole interface channel towards a low-Ohmic one at some well-defined threshold bias.

This behavior can be quantified after making the same set of assumptions as above. Let us draw our attention to the diode D_w below contact w and above the interface. D_w is characterized by the resistance R_{dw}, to which the resistance R_w of the track material above D_w has to be added to obtain the total resistance at contact w. Further let the potential in the channel above contact v, U_v, be fixed and let us not admit any external charge supply. As long as D_w is closed, the channel resistance R_c near D_w will be very high: R_c ? 1 and the channel current I_c will be near zero. Consequently the potential U_w below D_w is equal to U_v.

Now open D_w slightly by applying a voltage U_w. Then the diode equation: $I_w = fU_w^2$ applies (f being a proportionality

factor), and consequently the diode resistance becomes: $R_{dw} = U_w/I_w = 1/(fU_w) = C_w/(fQ_w)$, C_w being the diode capacity. The current I_w through the diode D_w enables the injection of a charge Q_w into the channel below D_w which consequently becomes conducting. Assuming that the channel resistance R_c decreases inversely with the number of inserted charge carriers: $R_c = a/Q_w(t)$ (with a being a proportionality factor), the total resistance in our region of interest, $R = R_w + R_{dw} + R_c$, is reciprocal to Q_w (as long as $R_c \gg R_w + R_c$). Hence, the current through both the diode D_w and the neighboring channel is $I_w = dQ_w/dt = U_c/[R_w + R_{dw}(t) + R_c(t)] \sim AQ_w(t)$, with A being another proportional factor (if R_w is not too large). This gives rise to a differential equation of the type: $dQ_w(t)/dt = AQ_w(t)$ with the well-known solution: $Q_w(t) = Q_0 \exp(At)$; Q_0 being a constant.

The exponential rise of Q_w, signifying a dramatic increase of the charge injection, also leads to an exponential increase of the electrical current $I(t) = \int Q_w(t)dt = I_0 \exp(At)$, i.e. to the onset of a short circuit. Hence the voltage U_w applied to the diode collapses: $U_w(t) = U_v - Q_w(t)/C_w$ unless the charge loss from the structure can be compensated sufficiently fast. Both the positive dI_w/dt and the negative dU_w/dt combine to a differential resistance dR/dt, of the type: $C_1 - C_2 \exp(At)$ – hence to a NDR, with C_1 and C_2 being constants. The strong charge injection into the interface-near channel signifies that the system goes from a high-Ohmic to a low-Ohmic state. Destruction of the device is prevented by designing a sufficiently large track resistance R_w and/or by adding an external protective resistance R_{ext} to the circuit. This enables the system to arrive at some new equilibrium state, with the NDR being an intermediate transitional effect. Upon decrease of the applied bias, there is another abrupt back-jump, possibly at a somewhat lower threshold voltage towards the original high-Ohmic interface channel state, so that both forward- and back-jumps may describe a hysteresis-like curve in the current/voltage diagram.

Such NDRs have meanwhile been observed for a multitude of TEAMS and TEMPOS systems (e.g. C_{60}-TEAMS, Ag-Carbamate-TEAMS, Nanographite-TEMPOS, Ag- and Au-NC-TEMPOS), so that one can consider this to be a general property of such ion-track-based structures. NDRs are desired effects as they enable one to construct, e.g. amplifiers and oscillators. NDRs can also result from instabilities of e.g. radiation-induced defects or latent ion tracks which act as transient traps for charge carriers [16]. Eventually, permanent repetitions of gradual charging and rapid discharging processes set on even by themselves in TEAMS structures upon application of some bias [17].

4. Network theory

The multitude of interconnected three-dimensional electrical pathways between nanoclusters and along ion tracks of TEAMS or TEMPOS structures constitute a challenge to apply network theory to describe such systems. This has been done for a number of examples [18]. It has turned out that the Barabasi–Albert approach [19], presenting the scale-free cumulative probability for nodes up to a given distance r around a preset origin, is most adequate for our purpose.

Consider first the current distribution around a contact on the surface of a non-porous insulating plate onto which metallic NCs have been deposited randomly. Then the cumulative probability for a jump of a charge carrier from one NC to another will be independent of the distance from the contact, r. To describe the current distribution around such a contact, the probability distribution has to be weighed with 1/r, as the resistance increases linearly with r – hence the current distributions will also follow a 1/r - type relation.

If, however, these NCs are not just deposited onto a featureless insulating plate but onto a planar structure with embedded ion tracks, the latter will serve as sinks for the NCs during their deposition, so that one will find more NCs within the tracks than in their neighborhood, where they will be depleted (this is a general statement and holds for both randomly and non-randomly distributed ion track distributions). Consequently the NC distribution will no longer be a random one in that case. This could indeed be verified; the cumulative probability distribution is lowered up to a specific distance which is characteristic for the mean free NC migration pathlength in the phase of their deposition.

As a consequence of this reduced probability distribution, also the electric current distribution will be reduced as compared with the original $\propto 1/r$ distribution. For the example chosen here (Ag-NC-TEMPOS at 2×10^8 cm^{-2} areal etched track density), the distortion of the Ag NC distribution by the mere existence of randomly distributed ion tracks on the SiO_2 layer leads to a reduction of the 1/1000 width (i.e. the distance around an electric contact within which an electrical current I_0 drops to $I_0/1000$ – hence the distance behind which any current becomes virtually negligible) of the radial current distribution from ~ 10 μm to ~ 1 μm. This is valid as well for tracks to which no potential is applied at all, as for tracks which have been put onto a bias which closes the track diodes.

However, in case that the track bias leads to track diode opening, new current pathways directed towards the silicon substrate through the tracks add to the already existing ones. This signifies a further decrease of the horizontal current probability distribution, and consequently a significant reduction of the 1/1000 width. Depending on the parameters that influence the current distribution (the density of both the NCs and the tracks, and the ratio of track to surface conductivity), 1/1000 width of 500 nm and less become feasible.

This information is important to estimate the minimum possible distance of contacts of TEAMS or TEMPOS structures, hence to estimate their minimum sizes at which they can operate without creating shortcuts among each other. It is also important to estimate the maximum

number of contacts per unit area in case of multicontact structures. Based on the present experience, it is estimated that a 3 lm Â 3 lm large TEMPOS structure could host up to $9 contacts if operating in reversed-bias (i.e. closed) track diode direction, but up to $36 contacts if operating in forward-biased (i.e. open) direction.

It is planned to expand these calculations to future compact three-dimensional electronic structures where charge carriers can jump along many parallel planes, and in between them. Such structures, though not yet existing, have already been proposed [20]. They could be based on a multitude of parallel insulating and conducting planes that are held together by perpendicularly oriented parallel carbon nanotubes (CNTs). Indeed, first steps towards such structures have already been made. Recently $50 to 100 nm £ large CNTs could be successfully integrated into TEMPOS structures, by letting them grow into etched tracks in SiO_2 on Si [21], and 3D CNT networks have been formed by plasma enhanced chemical vapour deposition within zeolithe and porous silica [22,23].

5. Conclusions

TEAMS and TEMPOS structures are ion-track-based electronic structures with a multitude of promising properties. In this paper, emphasize was put on some peculiarities and their mathematical description. On the one hand the genealogic correlation of these structures with MOS transistors was outlined, which leads to somewhat similar formulae and to amplifying properties. On the other hand, these structures frequently exhibit negative differential resistances which are very useful for practical applications. Finally, network theory is applied to estimate the minimum possible sizes of TEAMS and TEMPOS structures, and the maximum number of possible contacts per unit device area.

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